

FORM PTO-892
(REV. 3-78)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

SERIAL NO.

869851
458,507

GROUP/UNIT

2306

ATTACHMENT
TO
PAPER
NUMBER

15

NOTICE OF REFERENCES CITED

APPLICANT(S)

Hori et al.

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
*	A	4239980	12-80	Takanashi et al.	307	205	
*	B	4482985	11-84	Itoh et al.	365	226	
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG.	PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

*	R	Itoh, K., et al., "An Experimental 1Mb DRAM with On-Chip Voltage Limiter", <u>1984 IEEE International Solid-State Circuits Conf.</u> , pp. 282-283.
	S	
	T	
	U	

EXAMINER

Stephen Baker

DATE

1/14/92

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)